

ASIC Design Guidelines

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Introduction

- ASIC Design
 - Synchronous / Asynchronous
- Highlight specific design practices such as
 - unsafe
 - lead to devices difficult to test
 - can not guarantee its operation
- Suggestions of good design practice

Lecture in Brief

- Discussion of
 - A number of non-recommended Circuits
- Discussion of
 - Recommended (error free) circuits

Overview

- ASIC high design risk -- Working first time
- Delays in ASIC chip
 - Unpredictable before layout of the circuit
 - Can not be accurately calculated
- Clocking / clocking skew

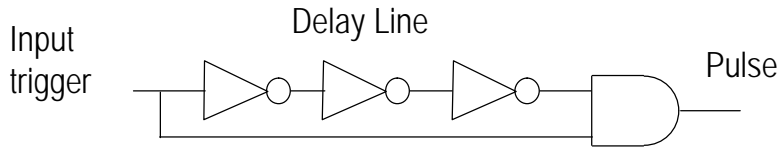
Signoff an ASIC Design

- Prior to submission for fabrication
- Customers must signoff a design to indicate
 - It complies with all the foundry set recommendations
- For each case on non-compliance
 - the case must be discussed with the foundry Design Centre
 - Obtain authorisation (if necessary)

Examples of Non-Recommended Circuits

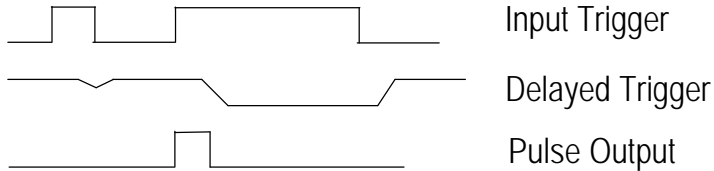
A delay circuit - Non-recommended

- To create a short pulse within a circuit of duration less than a clock cycle
- Example: A monostable element



Monostable Pulse Generator

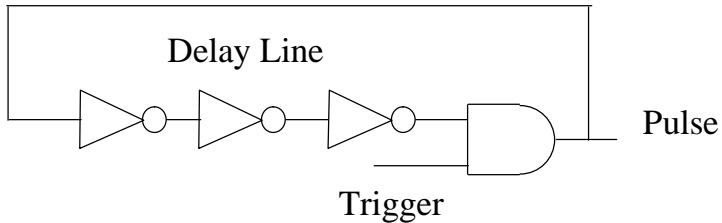
Monostable pulse generator



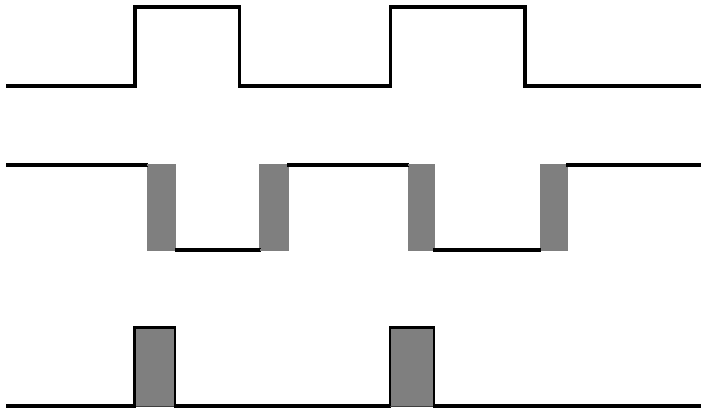
- It is not recommended -- It relies on delays for its operation (They are unpredictable in ASIC)
- Used in PCB -- Not suitable for ASIC

Multivibrator Circuits - 'Non-recommended'

- Avoid this type of circuit in ASIC
- Be careful, while designing the reset loop of a counter (found in synchronous circuits?)

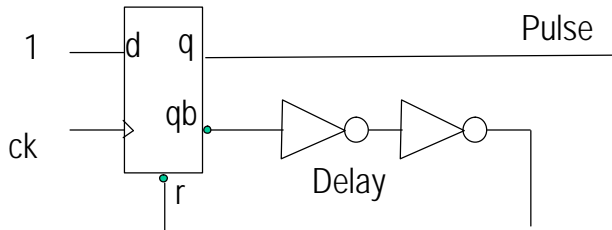


Multivibrator waveform



Another pulse generator Not recommended

- Pulse generator using D-type with reset input Flip-flop



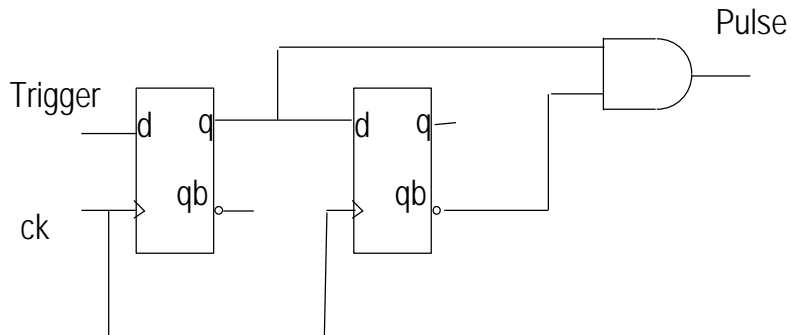
Delay Circuit Recommendations

- Avoid delay-line circuits if you can
- Discuss SPICE simulation results with the silicon foundry for authorisation
- Use higher clock speed.
 - Pulse width = clock cycle
- Use synchronous pulse generator

Recommended Pulse Generator

Synchronous Circuit

Synchronous Pulse Generator - Recommended



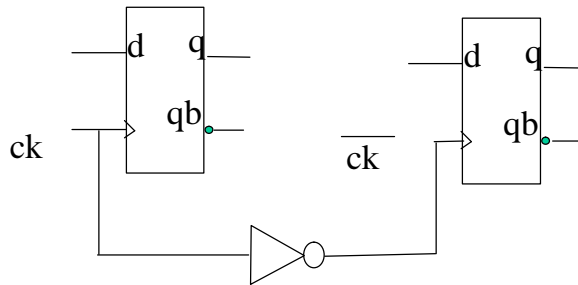
Synchronous pulse Generator

- Generate the waveform for this circuit
- Compare the pulse width with the clock cycle
- Compare this with the asynchronous multivibrator waveform

Clocked Counters and registers

Non-recommended Circuits

Some clocked circuits - Non recommended



Double-edged Clocking

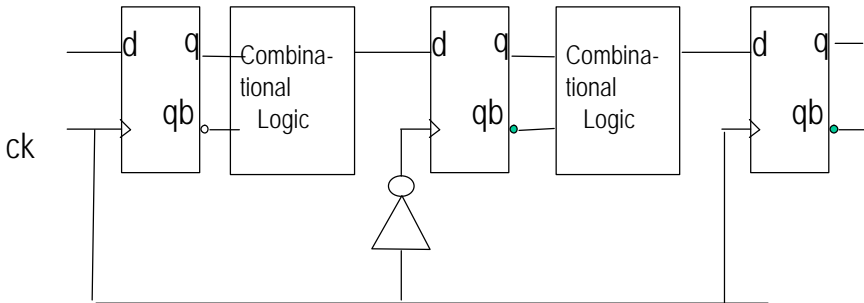
- Two flip-flops are clocked on opposite edges of the clock signal
- Makes synchronous resetting impossible
- Difficulties in determining critical signal paths
- Makes test methodologies such as scan-path insertion impossible (rely on all ff being activated on the same clock edge)

Double-edged Clocking

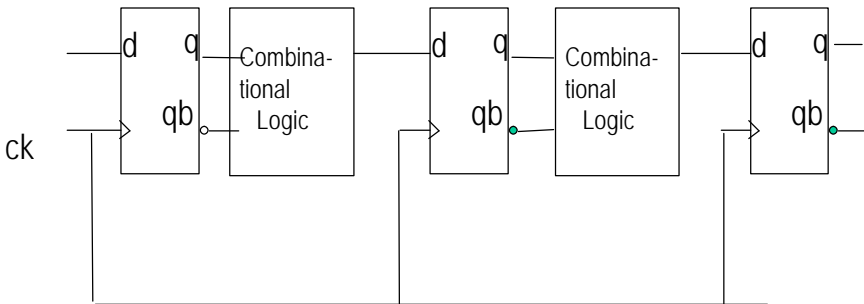
- This practice is
 - Required to increase data throughput rates
 - Use of both the rising and the falling clock edge for clocked elements
- An asymmetrical clock duty cycle can cause setup and hold violations
- Recommendation: use a single-edged clocking scheme with a higher clock frequency

Pipelined logic with double-edged clocking

Non-recommended

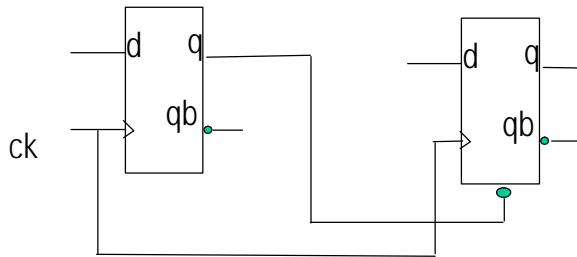


Pipelined logic with single-edged clocking - Recommended



Synchronous circuit -- Double the frequency
of the previous circuit

Asynchronous reset – Non recommended

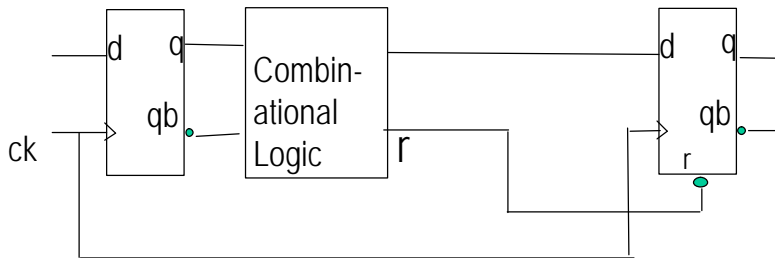


- Used as part of an asynchronously reset counter

Flip-flop driving asynchronous reset of another flip-flop ni2

- Violation of synchronous design. Second flip-flop can change state at a time other than the active clock edge
- Potential race condition between the clock and reset of the second flip-flop

Asynchronous reset Non-recommended



- Asynchronous reset causes a change of state on the second flip-flop which is not synchronous with the clock

Recommendations for asynchronous reset circuits

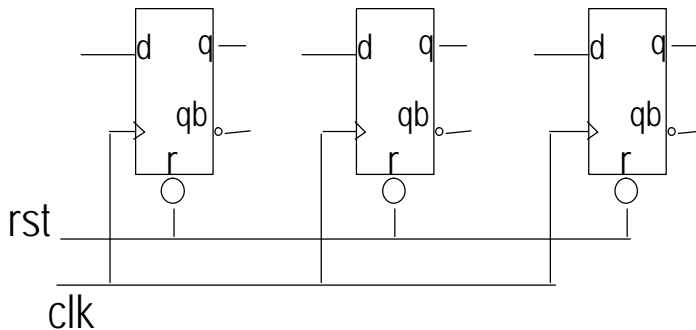


- Circuit must be brought to a known state within a stated and agreed number of clock cycles
 - This is achieved by a reset mechanism
 - Must be achieved during test and in operation
- Use a single global, external, asynchronous reset input to reset the entire circuit in a known state

Recommendations for asynchronous reset circuits

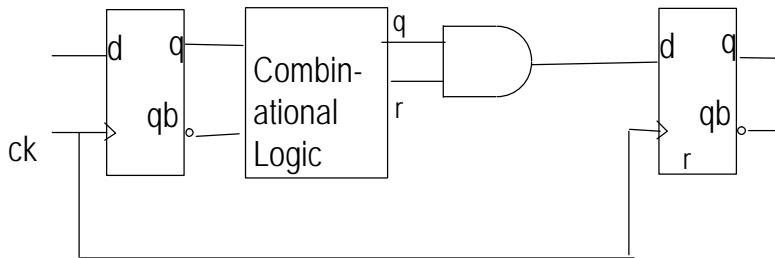
- Power on Reset (POR) pad (if implemented)! Also must contain another global reset for test
- For local reset use a synchronous reset
- Use balanced tree buffering, similar to clock buffering, to distribute reset signals

Recommended global asynchronous reset circuit



- A single reset 'rst' is connected to all flip-flops
- Buffering is needed for rst signal

Recommended local reset circuit

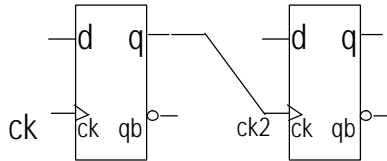


- Synchronous reset circuit -- reset is gated with 'd' input of second flip-flop

Gated Clocking

Non-recommended Circuits

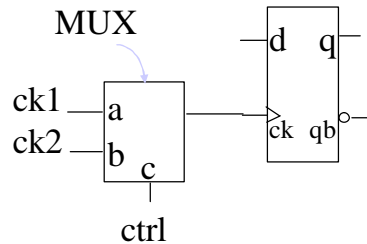
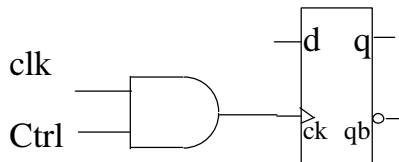
Flip-flop driving clock input of another – Non recommended



A ripple counter circuit

- ck2 is skewed by the clock-to-q delay of the first flip-flop
- flip-flop 2 is not activated on every ck edge

Gated clock - Non-recommended

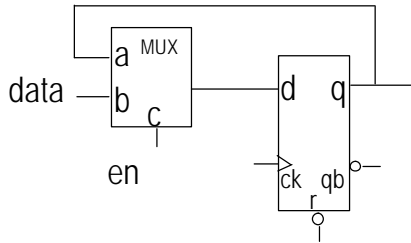


- clock skew due to gating
- Spikes / glitch problems

Recommended circuits

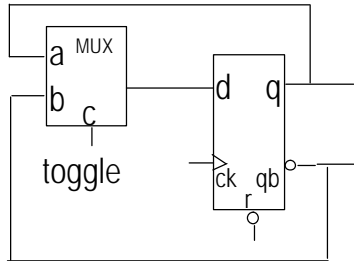
- Use synchronous design circuits based on
 - Enable E-Type flip-flop circuit
 - Toggle T-type flip-flop circuit
- Avoid gated clocks
- Avoid using the output from one flip-flop as a clock input to another

Synchronous Enable E-Type Flip-flop - Recommended



- Use system clock to gate data
- When $en = 0$ no change in q output
- When $en = 1$ data is clocked in

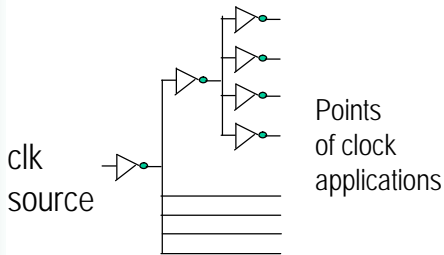
Synchronous Toggle T-Type Flip-flop - Recommended



- Basic element in synchronous counters
- When toggle = 0 no change in q output
- When toggle = 1 output data changes each clock cycle

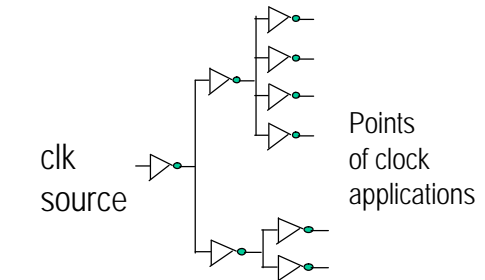
clock Buffering

Non-recommended buffering circuits



Cause clock skew

Unequal depth



Cause rise to different load-dependent delays -- clock skew

Unbalanced fanout

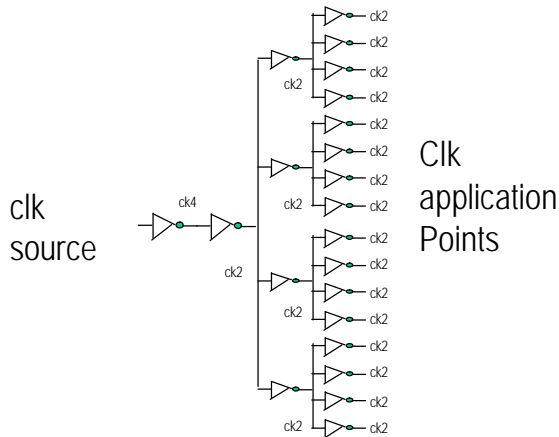
Non-recommended buffering circuits

- Excessive clock fanout
 - Cause slow clock edges
 - Increase risk of meta-stability in flip-flops capturing asynchronous signals
 - Turn the circuit from synchronous to asynchronous circuit

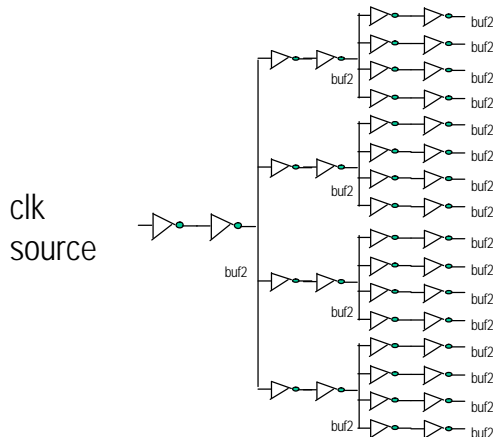
Recommended clock buffering circuit

- Use balanced tree buffering
 - Same depth of buffering to all clocked cells
 - Same fanout on all buffers
 - Tracking capacitances could unbalance the fanout -- Problem !!
 - must check after placement and routing
- To keep clock edges sharp
 - use lightly loaded buffers
 - Use a combination of geometric and tree buffering

Balanced clock tree buffering Recommended



Combined geometric & tree buffering -- Recommended



clk
source

Clk
application
Points

- Relative fanout is reduced at each buffer
- Sharp clock edges

buf2 = buffer with drive strength 2

Summary

- For ASIC -- Design safe -- Design synchronous
- Remember: ASIC is different from PCB
- Always follow the recommended path to ASIC
- Simulate and simulate and simulate