PLD Architecture

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AGENDA

- What is Programmable Logic?
- Basic Study Of XILINX CPLD Architecture – XC 9500.
- Basic Study Of XILINX FPGA Architecture – XC 4000.
- Comparison between FPGAs and CPLDs.

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Programmable Logic

- These are the devices with,
  - Programmable Interconnects.
  - Large number of flip-flops.
  - Large number of logic gates.
- Here memory cells controls the functionality through programmable interconnects.

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Types of Programmable Logic

- Simple Programmable Logic Devices(SPLDs)
- Complex Programmable Logic Devices(CPLDs)
- Field Programmable Gate Arrays(FPGAs)

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SPLDs

- SPLDs are simple programmable logic devices like,
  - PLA : Programmable Logic Array.
    - Contains AND and OR array.
    - AND array infers Product Terms for I/p variables.
    - OR array makes ORing of product terms to form output functions.
  - PAL : Programmable Array Logic
    - Here AND array is programmable and OR array is fixed.
  - GAL : Generic Array Logic.

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CPLDs

- These are having some higher logic capacity than SPLDs.
  - One typical CPLD may be equivalent to 2 to 64 SPLDs.
  - The development languages of most of the CPLDs and SPLDs are same like ABEL,CuPL,PALASM etc.
- Some of the CPLDs are,
  - EPLD – Erasable Programmable Logic Device.
  - PEEL – Programmable Electrically Erasable Logic.
  - EEPLD – Electrically Erasable Programmable Logic Device.
  - MAX – Multiple Array Matrix of Altera.

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CPLDs

- CPLD microcells consists of different Logic Blocks interconnected together via a programmable Switch matrix.
- A Function Block contains a group of 8 to 10 microcells grouped together.
- CPLD uses a non-volatile memory cells such as EPROM,EEPROM,FLASH.
- In circuit Programmability can be achieved by using ISP feature of CPLDs. (I.e. In System Programmable)

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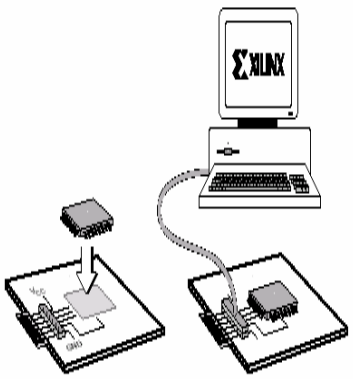
ISP



In system Programmable (ISP):

Means The ability to reconfigure the logic & Functionality of a device.

This can be done before,after or during the manufacture.

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ISP Features & Advantages

- Features of ISP :
  - Flexible and easy to modify hardware.
  - Design Up gradation is simple.
  - No special manufacturing flow is required.
  - 20-year program retention ability.
  - A minimum 10,000 program-erase cycles.
- Advantages of ISP :
  - Faster time to market.
  - Internal test and board reconfiguration.
  - Superior prototyping with multi function h/w designs.
  - Security feature allowing density security, I.e. A secured device can not be read back until it has been erased.

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FPGAs

- FPGAs are having
  - an internal array of Logic Blocks.
  - Surrounded ring of I/O Blocks.
  - Programmable Interconnects.
- These are also known as ,
  - LCA – Logic Cell Array.
  - ACT – Actel
  - FLEX,APEX – Altera
  - pASIC – Programmable ASICs-QuickLogic.
  - Virtex – XILINX
  - ORCA - Lucent

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FPGA Classification

- FPGAs are classified according to their Architecture as,
  - Coarse Grained
  - Fine Grained
- Coarse Grained Architectures are consists of some fixed high performance logic blocks like ALUs, registers, multipliers.

  Ex. Atmel (AT 40K),Altera (FLEX).
- Fine Grained Architectures are consists of Small Local Memories

  Ex. Actel ACT FPGAs.

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Manufacturing Technologies

- Most FPGAs use SRAM or Anti-Fuse CMOS Technology.
  - SRAM based FPGAs are programmable.
  - Anti-Fused based FPGAs are one time programmable.
- In SRAM technology Configuration Memory has a program in it that defines
  - The function of each logic block
  - Which blocks are I/ps and which are o/ps.
  - Interconnects between blocks.
- In anti-fuse technology, a programming current of 5 mA blows an anti-fuse to make a permanent connection.

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Advantages of Programmable Logic

- Saves valuable board space and debug time.
- Includes a security fuse that can be used to protect IP.
- Requires Less switching current and switching o/ps.
- Faster time to market.
- Less NRE cost with more logic flexibility.

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XC9500 in system Programmable CPLD Family

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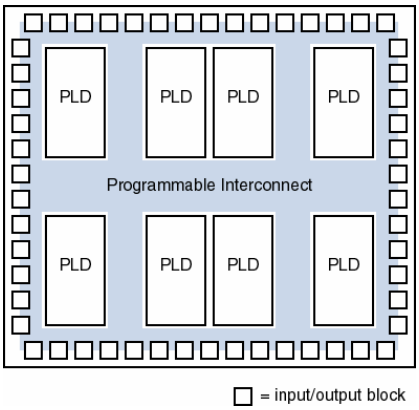
CPLDs

- Small number of largish PLDs (e.g., '36V18') on a single chip.
- Programmable interconnect between PLDs



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CPLD families

- Identical individual PLD blocks (Xilinx 'FBs') replicated in different family members.
  - Different number of PLD blocks
  - Different number of I/O pins
- Many CPLDs have fewer I/O pins than macrocells
  - "Buried"Macrocells -- provide needed logic terms internally but these outputs are not connected externally.
  - IC package size dictates # of I/O pins but not the total # of macrocells.
  - Typical CPLD families have devices with differing resources in the same IC package.

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Features

- High Performance
  - 5ns Pin to pin delays on all pins
- Large density range
  - 36 to 288 macro cells with 800 to 6400 usable gates
- 5 V in system programmable
  - Endurance of 10,000 program/erase cycles.
  - Program/erase over full commercial voltage and temperature range.
- Enhanced pin-locking architecture
- Flexible 36V18 function Block.
  - 90 product terms drive any 18 macrocells within function block.
  - Global and product term clocks, output enables, set and reset signals.
- Slew rate control on individual outputs.
- User programmable ground pin capability
- Advanced CMOS 5V FastFlash technology.

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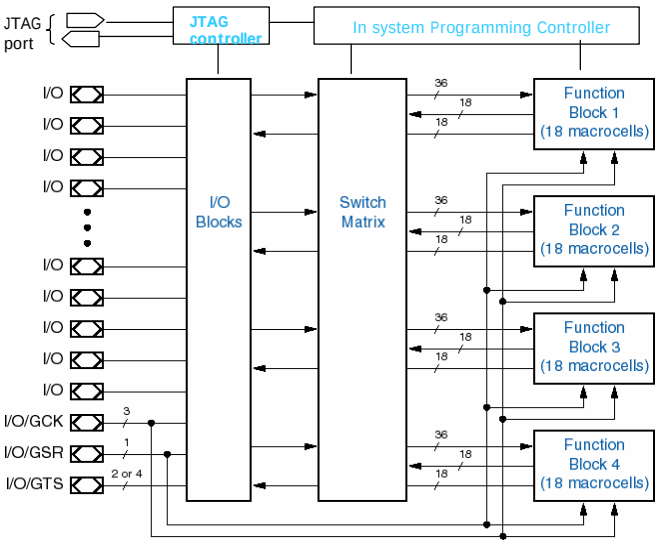
Architecture of XC9500



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Architecture Description

- Each XC9500 device is a subsystem consisting of multiple
  - Function Blocks (FBs)
    - Provides programmable logic capability with 36 inputs and 18 outputs.
  - I/O Blocks(IOBs)
    - The IOBs provide buffering for device inputs and outputs.
  - FastConnect switch matrix.
    - Connects all FB outputs and inputs signals to the FB inputs.

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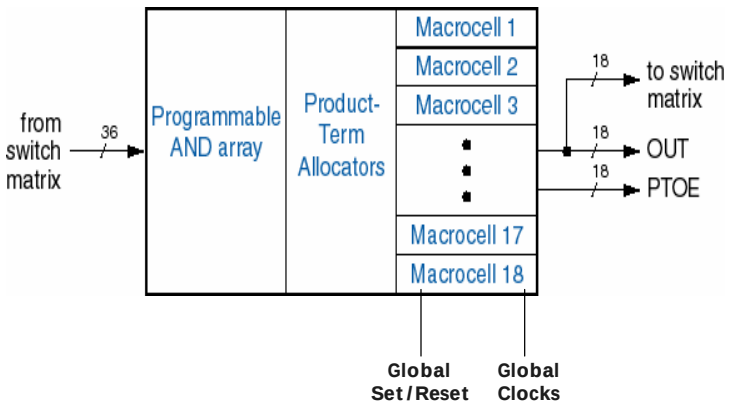
Function Block



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Function Block

- 18 macrocells per FB ,capable of implementing registered and combinatorial Logic.
- 36 inputs per FB , 72 true and complement signal into the programmable AND- array to form 90 product terms.
- Macrocell outputs can go to I/O cells or back into switch matrix to be routed to this or other FBs.
- Product Term Allocator allocates maximum 90 product terms to each microcell.

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Function Block

- The FB also receives global clock, output enable, and set/reset signals.
- The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.
- Logic within the FB is implemented using a sum-of-products representation.

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Function Block

- Thirty-six inputs provide 72 true and complement signals into the programmable AND-array to form 90 product terms.
- Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.
- Each FB (except for the XC9536) supports local feedback paths that allow any number of FB outputs to drive into its own programmable AND-array without going outside the FB.
  - These paths are used for creating very fast counters and state machines where all state registers are within the same FB.

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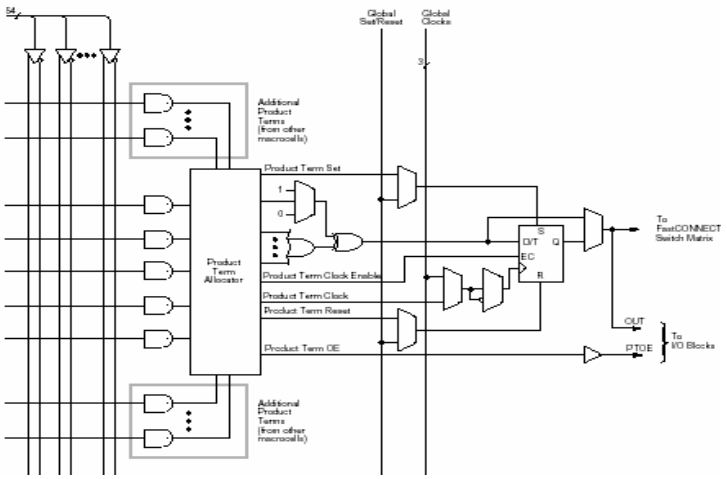
Macrocell



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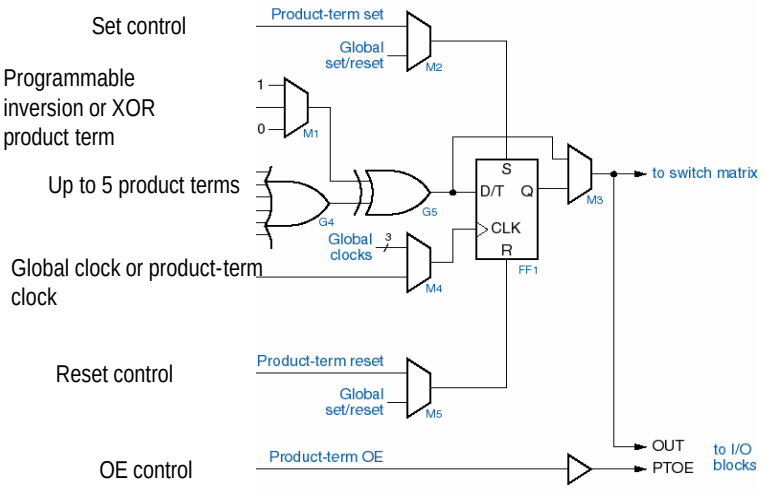
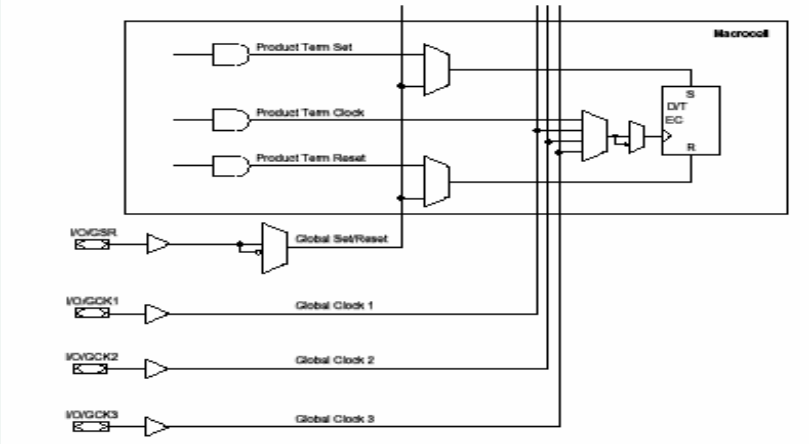
Macrocell

- Five product terms from AND-array are available for use of primary data inputs.
- The product term allocator associated with each macrocell selects the five direct terms are used.
- The register can be used as either D or T type F/F and supports both asynchronous set and reset operations.
- During Power-up,all user register are initialized to the user defined preload state(default 0)
- All global control signals available to each individual macrocell, including clock, set/reset,and output enable signal.

Macrocell



Macrocell Clock and Set / Reset Capability



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Global Control Signals

- In this device architecture there are some dedicated resources like Global Buffers, that are recommended for some high fanout nets which,
  - Reduce routing congestion.
  - Minimizes clock skew.
  - Route critical nets.
- Global control signals are:
  - Global Set/Reset(GSR)
  - Global Clock (GCK)
  - Global Tri-state Control (GTS)

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Clock Buffers

- These are basically used to reduce clock skew.
- These are used to,
  - Implement high-speed I/O interfaces.
  - Drive high fanout signals such as Clocks,read-write enables with minimum skew.
- These can also be applied to non-clock signals.

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GSR Buffers

- These are used to asynchronously SET or RESET F/Fs or RAM,Memory inside the device.
- Here external reset signal must be connected to GSR dedicated pin of XC9500.
- GSR can be programmed to either active-high or low.

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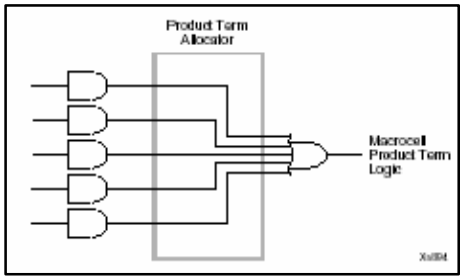
Product Term Allocator

- Controls how the five direct product terms are assigned to each Macrocell.
- Any Macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB.



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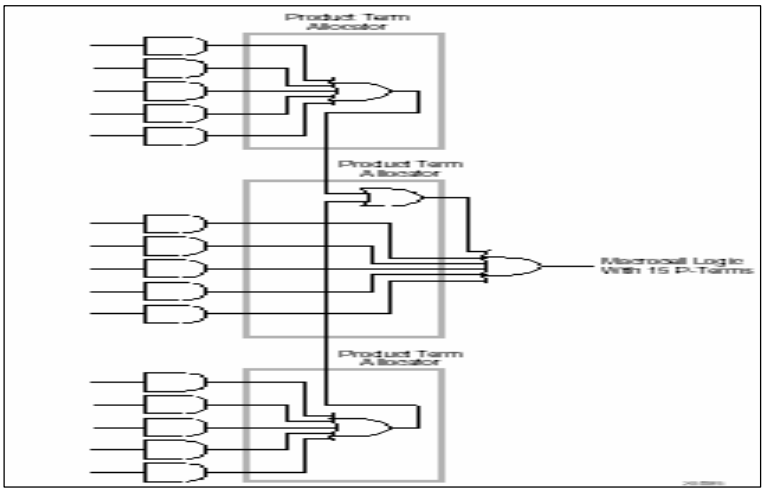
Product Term Allocator



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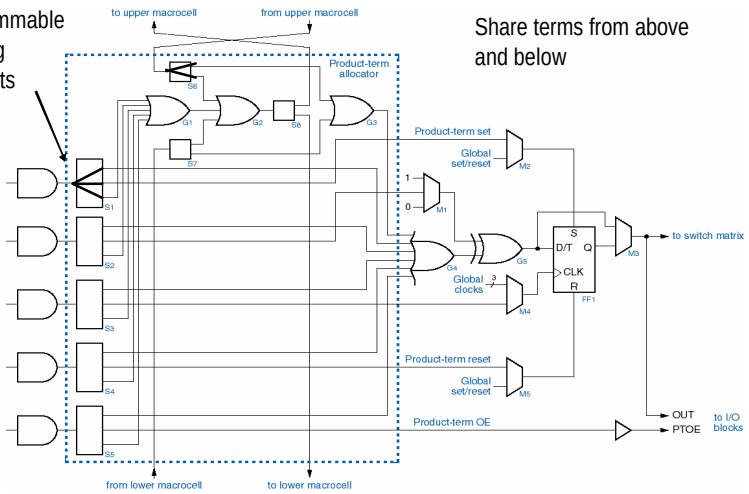
Product Term Allocator

programmable steering elements

Share terms from above and below



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FastConnect Switch Matrix

- The FastConnect switch matrix connect signals to the FB inputs.
- All IOB outputs and all FB drive the FastConnect matrix.
- Capable of combining multiple internal connections into a single Wired-AND output before driving the destination FB.
- This increase the Fan-in without additional time Delay.

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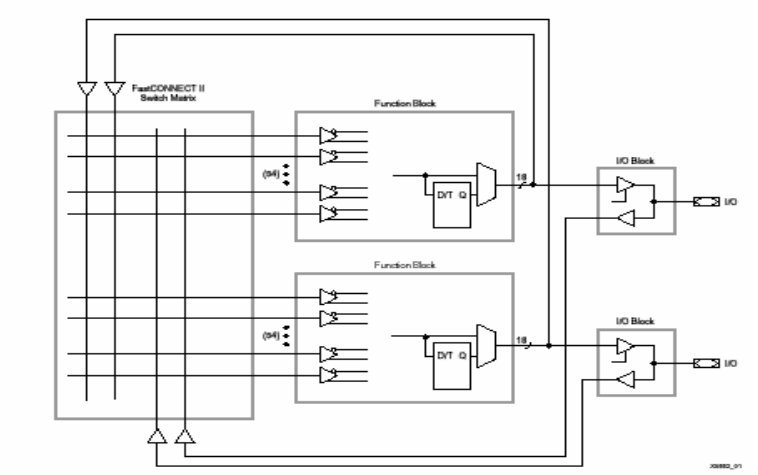
FastConnect Switch Matrix



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Interconnect structure

XC9500 CPLDs combine a locally efficient logic block with a globally flexible interconnect structure to provide ideal connectability for a very large spectrum of designs. The key qualities of the logic block are:

- 36 input signals presented to the logic block.
- Automatic allocation of product terms as needed within the function block. The average is 5 product terms per macrocell, but up to 15 are easily obtained and up to 90 can be used when needed.
- Formation of efficient counters, multiplexers, shifters, and parity circuits with an efficiency of one macrocell or less per bit. The remaining logic is available for use by other functions.

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Interconnect structure

The key properties of the interconnect structure are:

- Any input pin connects to any function block with constant high speed across the entire device.
- Any macrocell output can connect to its own or any other function block with no restriction.
- Macrocells can be internally bused with bit level independent 3-state control, to form internal data buses with global access to all logic blocks. (No other CPLD architecture offers this capability, which saves macrocell logic by using the routing resources to form multiplexers.)

These key features allow significant design changes to be made within CPLDs that are already attached to PC boards.

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I/O Block

- Interfaces between internal Logic and I/O Pins.
- IOB consists of an
  - Input Buffer
    - Compatible with standard 5V volt CMOS, 5VTTL and 3.3 V signal levels.
  - Output Driver
    - Capable of supplying 24 mA output drive.
  - Output enable selection multiplexer
    - Can be generated from, A product term signal, Any of the global OE signals
  - User programmable ground control
    - To reduce system noise generated from large number of simultaneous switching outputs.

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I/O Block

- A control Pull-up resistor is attached to each device I/O pin to prevent them from floating
- The resistor is Active during device programming, System Power-up and erased device.
- Deactivated in normal operation
- Independent Slew rate control. Output edge rate may be slow down to reduce noise through programming.

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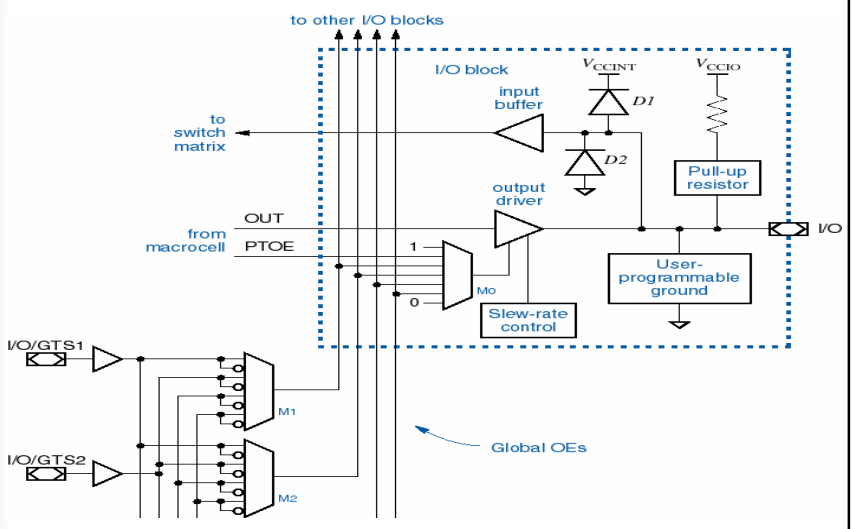
I/O Block



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Pin Locking

- The capability to lock the user defined Pin assignments during design changes depends on the ability of the architecture to adapt to unexpected changes.
- Small changes, and certainly large ones, can cause the fitter to pick a different allocation of I/O blocks and pinout.
- Locking too early may make the resulting circuit slower or not fit at all.

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Pin Locking

- To address the pin locking issues XC 9500 provides
  - Routing resources
    - Primary requirement for reliable pin-locking.
  - Function Block Fan-in capability
  - Product Term Allocation
  - Fitter Strategy

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Technology Used

- CPLD's are non-volatile devices, I.e retain the program after Power-off.
- The EPROM, EEPROM, FastFlash are the non-volatile type of memory.
- The FastFlash technology is used because of its advantage over the EEPROM.
  - High Performance Logic Device.
  - High Memory cell density
  - Electrical erasable
  - 5 V program and erase
  - High reliability and endurance
  - Process scalability
  - Fast device programming times

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Endurance limits

- The number of times that a cell can be programmed and erased without any error is called Endurance.
- The devices of XC9500 series have a minimum endurance limit of 10,000 cycles.

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FPGA 4000e Series


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AGENDA

- FPGA Architecture – XC 4000E
- Programmable Interconnects.
- Architectural Resources.
- Power Distribution in an FPGA.
- Configuration.


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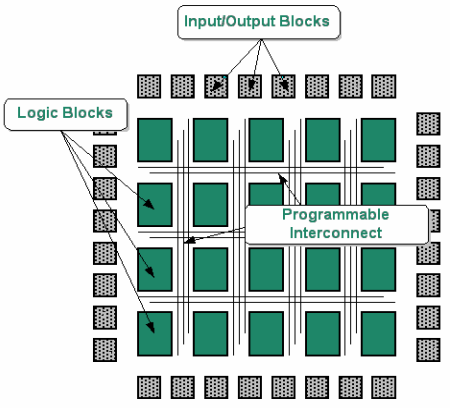
FPGA Architecture

- Much larger number of smaller programmable logic blocks.
- Embedded in a sea of lots and lots of programmable interconnect.



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FPGAs

- Historically, FPGA architectures and companies began around the same time as CPLDs.
- FPGAs are closer to "programmable ASICs"-- large emphasis on interconnection routing
  - Timing is difficult to predict -- multiple hops vs. the fixed delay of a CPLD's switch matrix.
  - But more "scalable" to large sizes.
- FPGA programmable logic blocks have only a few inputs and 1 or 2 flip-flops.

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Xilinx 4000-series FPGAs

Device	CLB Matrix	Total CLBs	Max. User I/O	Flip-Flops	Max. RAM bits (no logic)	Max. Gates (no RAM)	Typical Gate Range (Logic and RAM)
XC4002XL	8×8	64	64	256	2,048	1,600	1,000–3,000
XC4003E	10×10	100	80	360	3,200	3,000	2,000–5,000
XC4005E/XL	14×14	196	112	616	6,272	5,000	3,000–9,000
XC4006E	16×16	256	128	768	8,192	6,000	4,000–12,000
XC4008E	18×18	324	144	936	10,368	8,000	7,000–15,000
XC4010E/XL	20×20	400	160	1,120	12,800	10,000	7,000–20,000
XC4013E/XL	24×24	576	192	1,536	18,432	13,000	10,000–30,000
XC4020E/XL	28×28	784	224	2,016	25,088	20,000	13,000–40,000
XC4025E	32×32	1,024	256	2,560	32,768	25,000	15,000–45,000
XC4028EX/XL	32×32	1,024	256	2,560	32,768	28,000	18,000–50,000
XC4036EX/XL	36×36	1,296	288	3,168	41,472	36,000	22,000–65,000
XC4044XL	40×40	1,600	320	3,840	51,200	44,000	27,000–80,000
XC4052XL	44×44	1,936	352	4,576	61,952	52,000	33,000–100,000
XC4062XL	48×48	2,304	384	5,376	73,728	62,000	40,000–130,000
XC4085XL	56×56	3,136	448	7,168	100,352	85,000	55,000–180,000

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Features

- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option.
    - dual-port RAM option
  - Fully PCI compliant (speed grades -2 and faster)
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks.

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Features

- System Performance beyond 80 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per XC4000E output
- Configured by Loading Binary File
  - Unlimited re-programmability.

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Basic Building Blocks

- Xilinx user-programmable gate arrays include two major configurable elements:
  - Configurable logic blocks (CLBs):
    - CLBs provide the functional elements for constructing the user's logic.
  - input/output blocks (IOBs).
    - IOBs provide the interface between the package pins and internal signal lines.

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Basic Building Blocks

- Three other types of circuits are also available:
  - 3-State buffers (TBUFs) driving horizontal longlines are associated with each CLB.
  - Wide edge decoders are available around the periphery of each device.
  - An on-chip oscillator is provided.
- Programmable interconnect resources provide routing paths to connect the inputs and outputs of these configurable elements.

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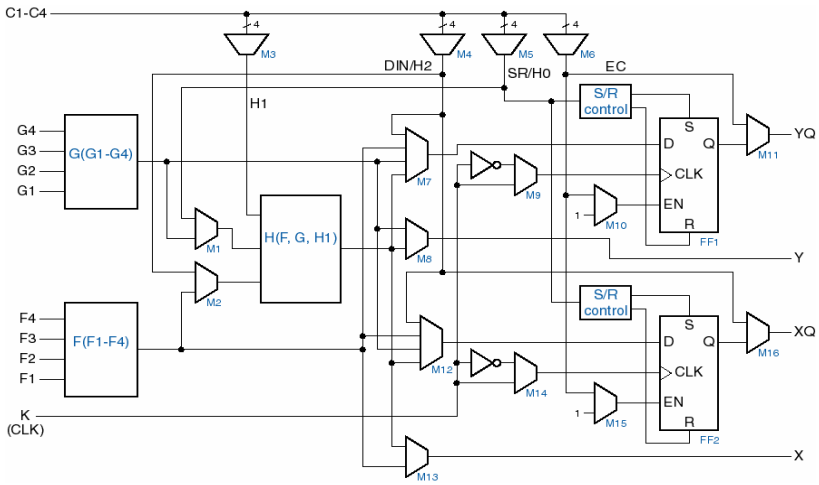
Configurable Logic Blocks (CLBs)



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CLB function generators (F, G, H)

- Use RAM to store a truth table
  - F, G: 4 inputs, 16 bits of RAM each(function Generator)
  - H: 3 inputs, 8 bits of RAM (function Generator)
  - RAM is loaded from an external PROM at system initialization.
  - Each CLB contains two storage elements that can be used to store the function G.
  - So main advantage here is function generator and storage elements both can be used independently.
  - Here each f/f can be triggered either on positive or negative clock edge due to combination of multiplexer and an inverter.
  - Each f/f can be configured to be SET or RESET using (SR).

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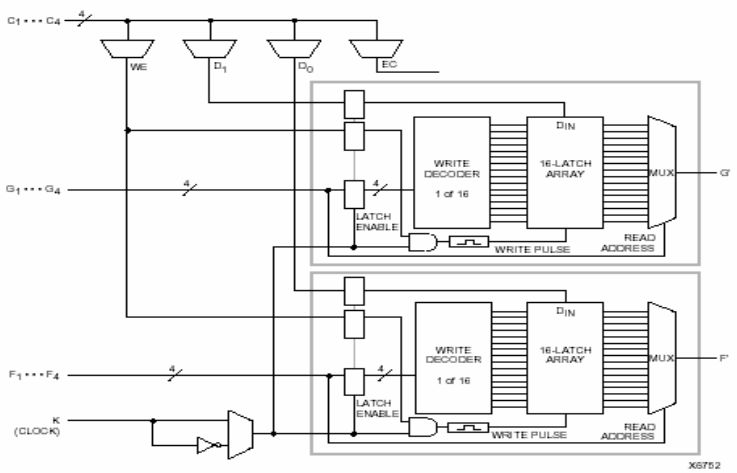
Using Function Generators as RAM

- 16x2 (or 16x1) Edge-Triggered Single-Port RAM



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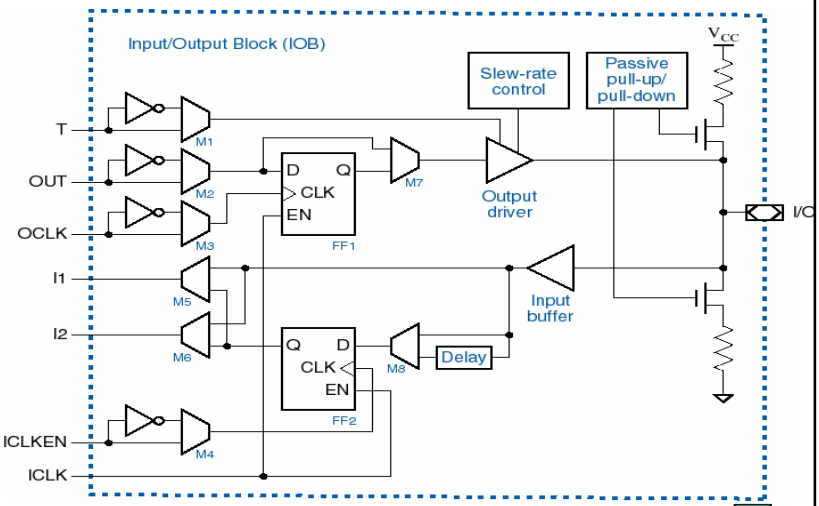
Input/Output Blocks (IOBs)



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Input/Output Blocks (IOBs)

- Input/Output Blocks :
  - Provide the interface between external package pins and the internal logic.
  - Each IOB controls one Package pin and can be configured for input, output or Bi-directional signals.
  - Input signals also connect to an input register that can be programmed as either an edge or level triggered.
  - Output signal can pass directly to the pad or be stored in an edge triggered flip-flop.
  - Slew rate control is used to avoid noise, Passive PU and PD are used to connect the IOB to either VCC or GROUND permanently.

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Input/Output Blocks (IOBs)

- IOB options :
  - Programmable Pull-up and Pull-down resistors are useful for tying in used pins to V_{CC} or ground to minimize power consumption and reduce noise sensitivity.
  - Separate clock signals are provide for input and output flip-flops.
  - JTAG support
  - Embedded logic attached to the IOBs contain test structures for boundary scan testing, permitting easy chip and broad level testing.

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Architectural Resources

- Storage Elements
  - Like Flip-Flops and Latches
  - Gives Pipelined Designs.
- RAM using Function Generator
  - Each CLB makes the memory look up tables in 'F' and 'G' function generators and can be used as an array of Read/Write memory cell depending on the selected operational mode.
  - Operational modes are level-sensitive, edge triggered and dual-port-edge triggered.
  - Depending upon the selected mode the CLB can be configured as either a 16x2 ,32x1 or 16x1 bit array.

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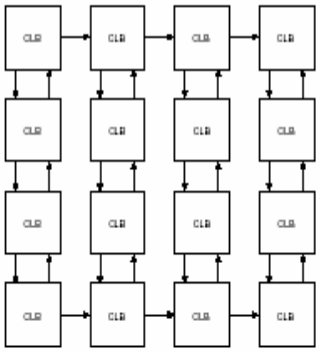
Architectural Resources

- Fast Carry Logic
  - There is a dedicated arithmetic logic for the fast generation of carry and borrow signals in each CLB's F and G function Generators.
  - Carry chain is used for fast carry logic which is independent of normal routing resources.
  - Between each CLB there are 8 permanent connections i.e. carry chain.
  - This fast carry logic greatly increases the efficiency and performance of adders,counters

    subtractors, accumulators and comparators.



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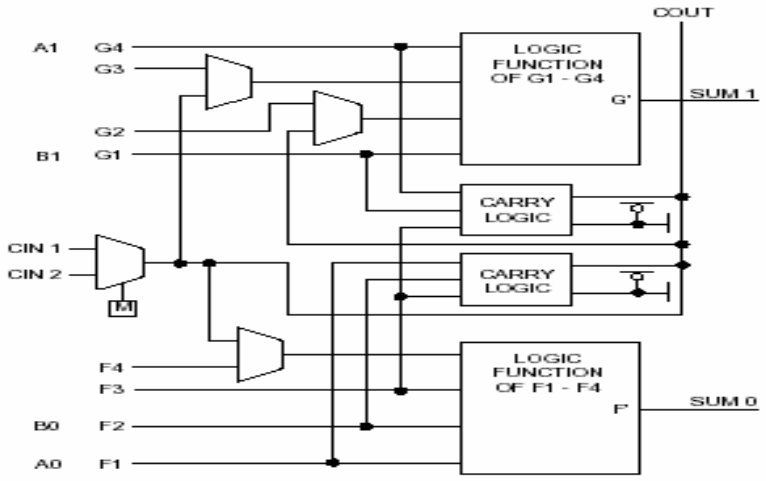
Fast Carry Logic



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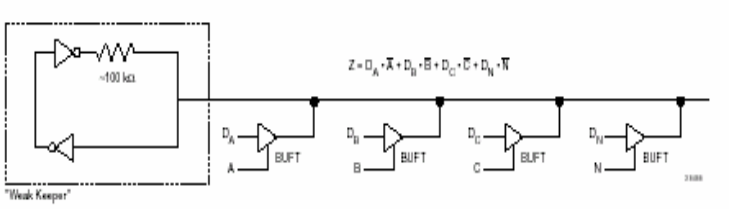
Architectural Resources

- Tri state buffers
  - A pair of 3-state buffers is associated with each CLB in the array.
  - These can be used to implement multiplexed or bidirectional buses on the horizontal longlines to save other logic resources.
  - Programmable pull-up resistors attached to these longlines help to implement a wide wired-AND function.
  - Week Keeper avoids data contention while writing data and latches previous value.



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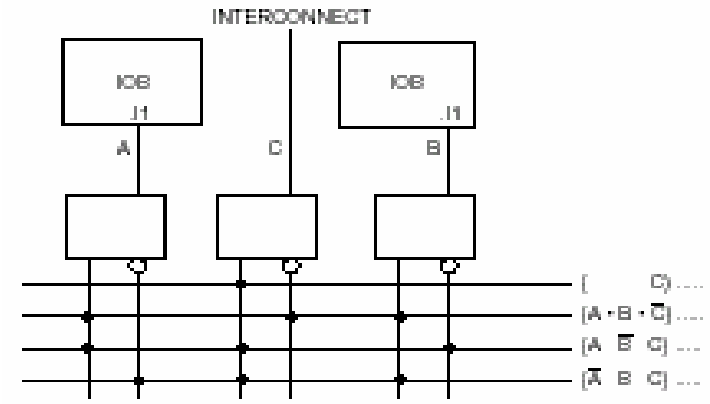
Architectural Resources

Wide edge decoders



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Architectural Resources

- Wide edge Decoders:
  - Used to decode specific values from a large number of bits e.g address decoding of large microprocessors
  - These are separate from CLB and do not use CLB resources.
  - These are implemented as wired AND gates.
  - Four programmable decoders are located on each edge of the device.
  - Each row or column of CLBs provides up to three variables or their compliments.
  - Each decoder generates a high o/p(Resistive Pull-up) when the AND gate condition is TRUE.

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Architectural Resources

- On-Chip Oscillator:
  - It is used to clock the power-on time-out for configuration memory clearing and as the source of CCLK in master configuration modes.
  - The counter runs at 8Mhz nominal frequency which varies with VCC and temperature. The o/p frequency falls between 4 to 10Mhz.
  - On chip clock is available to load the data from EPROM to configuration memory.

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Programmable Interconnects

- All internal connections are composed of metal segments with programmable switching points and switching matrices to implement the desired routing.
- Interconnections between two CLBs is not fixed and can take any path through switch matrix so that the delays can not be exactly predictable in FPGAs.
- Programmable interconnects between CLBs and IOBs can be made by,
  - General purpose interconnects between CLBs
  - Direct Interconnects
  - Long Lines

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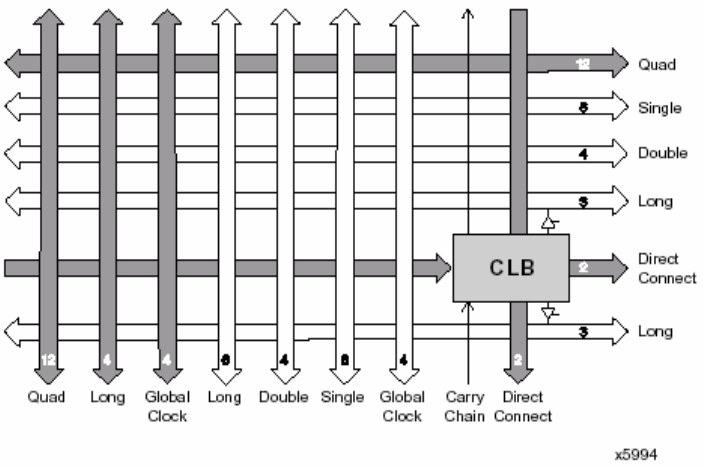
Programmable Interconnects



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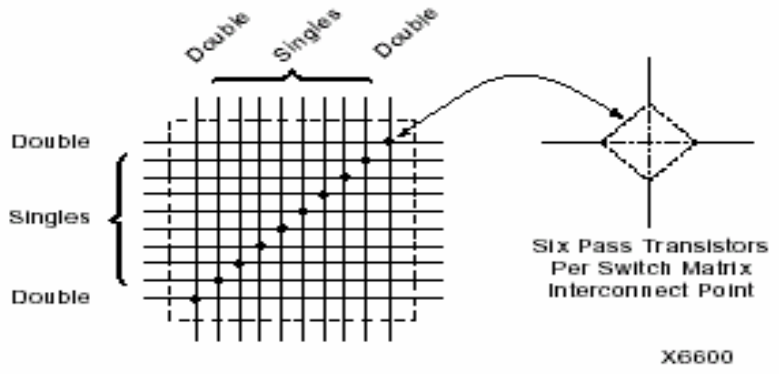
Programmable Interconnects

- At a time two paths can be active by choosing the vertical & horizontal lines



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Programmable Interconnects

	XC4000E		XC4000X	
	Vertical	Horizontal	Vertical	Horizontal
Singles	8	8	8	8
Doubles	4	4	4	4
Quads	0	0	12	12
Longlines	6	6	10	6
Direct Connects	0	0	2	2
Globals	4	0	8	0
Carry Logic	2	0	1	0
Total	24	18	45	32

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Programmable Interconnects

- Long lines runs
  - Entire width of the array
  - Are intended for high fanout and time critical signal nets.
- Each logic cell has two adjacent tri-state buffers that connect to horizontal long lines.
- Long lines and buffers can be used to implement tri-state buffers.

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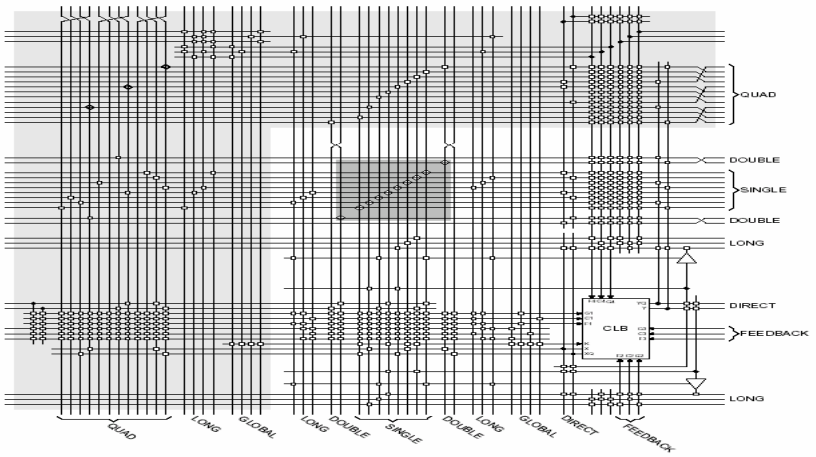
Programmable Interconnects



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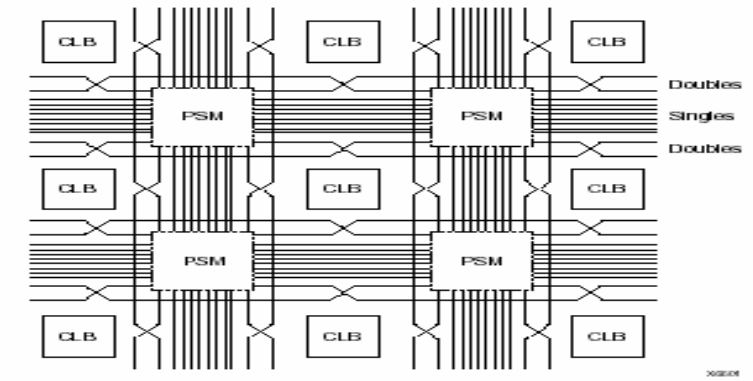
Programmable Interconnects

Signals between CLBs & IOBs can routed through switch matrix.



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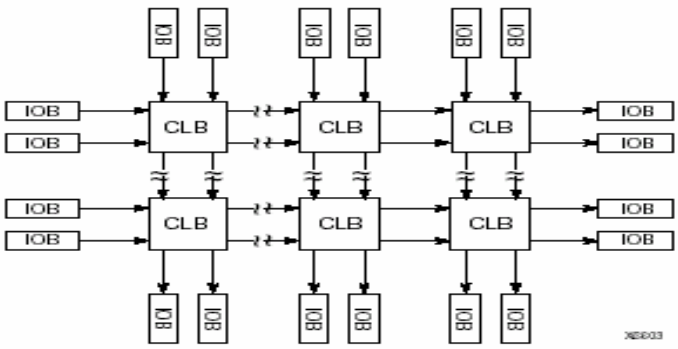
Programmable Interconnects

Direct Interconnects:

- Gives direct & efficient interconnects, Signals has minimum interconnect propagation delay.There is no use of general routing resources.



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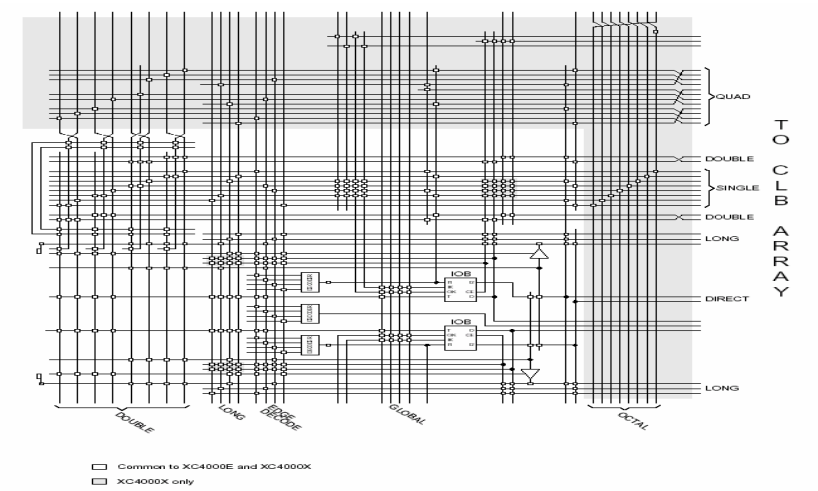
Programmable Interconnects



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Interconnect overview

- General purpose interconnects join Switch matrices,Global nets and buffers.
- Vertical and horizontal lines run between CLBs.
- Long lines runs across the chip. Internal busses and tri-state buffers next to each CLB can be formed using Long lines.
- Programmable Interconnect Points (PPIs) are programmable pass transistors that connect CLB inputs outputs to routing network.
- Bi-directional Interconnect Buffers (BIDI) restore the logic level and logic strengths on long interconnect paths.

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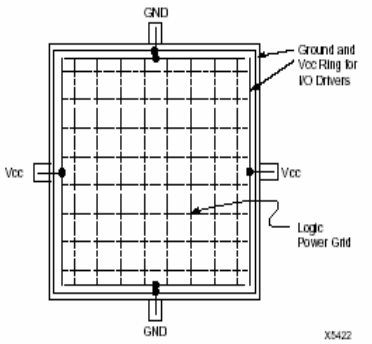
Power Distribution In FPGA

- Power is distributed through a grid to achieve high noise Immunity and isolation between logic and I/O.
- Dedicated Ground and VCC ring surrounding the logic array provides power to I/O drivers.
- An independent matrix of VCC and Ground supplies the internal logic of the device.
- Typically 0.1 microfarad capacitor is connected between VCC and Ground for de-coupling.



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Configuration

- Configuration is a process of
  - Loading a specific programming data to a FPGA.
  - To define the functional operation of the internal blocks and their interconnects.
- Special Purpose Pins for Configuration :
  - Dedicated Pins
  - Special function User I/O Pins
  - Un restricted user programmable I/O Pins.

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Configuration

Dedicated Pins:

- CCLK : Acts as a configuration clock.Internal oscillator generates CCLK.Its selected as 1MHz(default) or 8MHz.
- DONE : It's a bi-directional signal and indicates completion of a configuration process.
- PROGRAM : Clears FPGA configuration memory and initiates configuration cycle.
- VCC : Eight or more connections to nominal 5V supply.
- GND : Eight or more connections to nominal ground.

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Configuration

Special function user I/O Pins :

- M0, M1, M2 : Used for configuration mode selection.
- INIT : A bi-directional signal used to delay the configuration. A low on this pin indicates that configuration data error has occurred.
- A0 to A17 : These pins address the configuration EPROM during Master Parallel configuration.
- D0 to D7 : Receives configuration data during Master Parallel and Peripheral modes
- DIN : Serial configuration data input that receives data on the rising edge of clock.
- DOUT : Serial configuration data output. In daisy chaining acts as a DIN for next FPGA in chain.
- TDI, TDO, TMS, TCK : Pins for Boundary scanning or as I/O if not used for boundary scanning.

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Configuration

Unrestricted User-Programmable I/O Pins :

- Special function user I/O pins can be used as user programmable I/Os after configuration.
- All outputs not used for configuration process are tri-stated with a 50K-100K pull-up resistor.
- After configuration if an IOB is unused then it is configured as an input with a 50K-100K Pull-up resistor.

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CPLD Vs FPGA

- Interconnect structure.
- In-system performance.
- Performance prediction.
- Logic Utilization.
- Process Migration.
- Applications.

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Interconnect Structure

- CPLD uses a Continuous interconnect structure :
  - Consists of metal lines of uniform length traverse the entire length and width of the device.
  - Since the resistances and capacitances of all interconnect paths is fixed, delays between any two logic cells can be predictable.
  - This minimizes the logic skew.
- FPGA uses a segmented interconnect structure.
  - Consists of matrix of metal interconnects that run throughout the device. Switch matrices or Antifuses join the ends of these segments allowing signals to travel between logic cells.
  - Number of segments required to interconnect signals is neither constant nor predictable, so delays are not fixed or specified until place and route is completed.

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In-System Performance

- In CPLDs,
  - Delays are not cumulative.
  - The delay is independent of the path the signal takes.
- In FPGAs,
  - Segmented interconnect delays are cumulative.
  - As the number of interconnect segments increases, the interconnect delay also increases.
  - No guarantee that the signals take the same path every time to reach its destination.
  - Signal skew and performance degradation becomes more prevalent as more interconnect segments are used, insufficiently routing signals through the device.

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Logic Utilization

- Logic cells in most FPGA architecture have fine granularity, therefore more logic cells are required to implement a function in FPGA than in a CPLD.
- Logic cells in FPGA can contain only small portion of a design, so a heavy burden is placed on its segmented interconnect structure.
- As design complexity increases, the probability of routing conflicts also increases leading to lower FPGA device utilization.
- Logic density in FPGA is less due to only 9 variables, where as CPLD has 36 variables available.

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Process Migration - CPLD

- PLD technology is measured in microns and metal layers.
- 'Micron" represents smallest dimension of a transistor within the device.
- Metal layers represents the number of levels in which metal is deposited in the device.
- CPLD's continuous interconnect structure requires few transistors to connect to logic cells.
- CPLD architectures are metal optimized and benefit more from process migration to Triple-Layer Metal (TLM).
- DLM – Dual Layer Metal , TLM – Triple Layer Metal.

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Process Migration - FPGA

- A segmented interconnect structure of FPGA contains relatively few metal segments that must pass through various transistors to connect logic cells.
- Number of switches(transistors) in FPGAs is more than CPLD so flexibility is more But there is limitation on size reduction.Due to this FPGAs can take less benefit from TLM process migration.
- Reducing the die size transistor size from 0.8 micron to 0.6 micron shrinks FPGA die size.However migrating from DLM to TLM does not create additional layers. So die size of FPGAs remains relatively constant.
- FPGAs can create a pyramid-like TLM structure with most area still on bottom layer.
- Very few FPGA vendors use a 0.6 micron TLM process.

Applications - FPGAs

- FPGAs :
  - Basically register intensive applications.
  - Data paths.
  - Hardware Emulation.
  - JTAG applications.
  - Image controller.
  - Battery powered applications.
  - Field-test equipments.
  - Gate-array prototyping.

Applications - CPLDs

- CPLDs :
  - Basically combinatorial functions.
  - Bus interfacings.
  - Comparators.
  - High-speed wide decoders.
  - Large fast state micro controllers.
  - High speed GLUE Logic.
  - System video controller.
  - PAL integration.