

VHDL Coding Format of *ni2designs*

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-- Title           : VHDL Coding Style
-- Project         : Sample code
-- File            : VHDL_Coding_Style.vhd
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-- Organization    : ni logic Pvt. Ltd., Pune, India
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-- Description     : D F/F with both O/Ps
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-- Notes           : To demonstrate and Standardized
--                 : VHDL coding style "ni2designs"
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library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;
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entity coding is
generic(rst_state:std_logic:= '1');      -- Active HIGH Reset
  Port ( rst : in std_logic;              -- reset
        clk : in std_logic;              -- clock
        d   : in std_logic;              -- data I/P
        q,q_bar : out std_logic); -- Q and Q bar O/Ps
end coding;
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architecture Behavioral of coding is
signal q_s : std_logic;                  -- define internal signals here &
                                          -- name them according to their function

begin
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----- Process for storing Data -----
process(rst,clk)
begin
if(rst = rst_state)then
  q_s   <= '0'
elsif( clk'event and clk = '1')then
  q_s   <= d;
end if;
end process;
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q      <= q_s;

q_bar  <= not q_s;

end Behavioral;
```

Note: For ni2 designers, put notes as much as possible, but don't create mess. And submit updated source file to your project manager.