Introduction to RISC Processor

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AGENDA

- What is RISC & its History
- What is meant by RISC
- Architecture of MIPS-R4000 Processor
- Difference Between RISC and CISC
- Pros and Cons of RISC
- Why RISC

What is RISC and its History

- RISC stands for
- “ Reduced Instruction Set Computer”.
- The IBM was the first company to define the RISC architecture in the 1970s.
- This research was further developed by the universities of Berkeley and Stanford to give basic architectural models.

What is RISC and its History

- RISC can be described as a philosophy with three basic levels :
- All instruction will be executed in a single cycle.
- Memory will only be accessed via load and store instruction.
- All executions units will be hardwired with no micro coding.

What is meant by RISC

- The instruction set is the hardware “language” in which the software tells the processor what to do. Surprisingly, reducing the size of instruction set -- eliminating certain instructions based upon a careful quantitative analysis, and requiring these seldom - used instructions to be emulated in software -- can lead to higher performance.
- For several reasons :

What is meant by RISC

- Some of the uses for the space :
- Additional registers.
- on-chip caches which are are clocked as fast as the Processor.
- Additional functional units for superscalar execution.
- On-chip support for floating-point operations.
- Increased pipeline depth.
- Branch prediction.
- Additional “non-RISC”(but fast) instructions.

What is meant by RISC

- The vacated area of chip can be used in ways that accelerate the performance of more commonly used instructions.
- It becomes easier to optimize the design.
- It allows MP to use techniques hitherto restricted to the largest computers.

What is meant by RISC

- Basically the philosophy is, that instructions are handled in parts:
  - Fetch the instruction.
  - Get the arguments
  - Perform the action
  - Write back the result

What is meant by RISC

- Another view point was that processors currently use a 32-bit data bus anyway, so why not make every instruction 32-bits wide? Every instruction cycle fetches 32-bits anyway.
- Using these 32-bits efficiently makes it logical, to use one byte to code the actual instruction and the other three bytes, to code the registers to act on. This makes using triadic instruction logical:

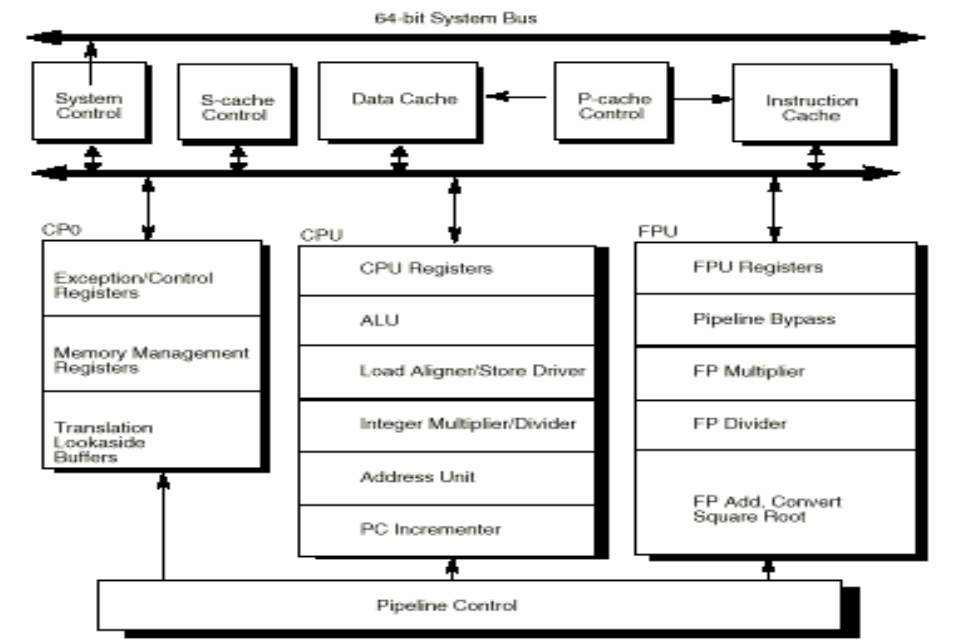
What is meant by RISC

- For example:
  - " add ro,r1,r2"
  - which means : r0 = r1 + r2.

RISC characteristics

- Simple instruction set.
- Same length instructions.
- 1 machine-cycle instructions.

R4000 Internal Block Diagram



MIPS-R4000 Processor

- Processor General Features :
  - CPU Overview
  - Register and Inst. Set Overview
  - Efficient pipeline.
  - Memory Management Unit (MMU).
  - Memory Organization.
  - System control coprocessor (CP0).
  - Floating - point Unit (CP1).

64 - Bit Architecture

- The R4000 processor contains 32 general purpose 64-bit registers.
- The natural mode of operation for the R4000 processor is as a 64-bit MP; however, 32-bit applications maintain compatibility even when the processor operates as a 64-bit processor.
- All instructions are 32 bits wide.

64-Bit Architecture

- The R4000 processor provides the following :
- 64-bit on-chip floating point unit(FPU).
- 64-bit integer arithmetic logic unit(ALU).
- 64-bit integer registers.
- 64-bit virtual address space.
- 64-bit system bus.

CPU Register Overview

- The CPU provides the following registers :
- 32 general purpose register.
- A program counter(PC) register.
- 2 registers that hold the results of integer multiply and divide operations(HI & LO).
- The R4000 has no Program Status Word(PSW) register, as such this is covered by the status and cause registers incorporated within the system control coprocessor(CP0).

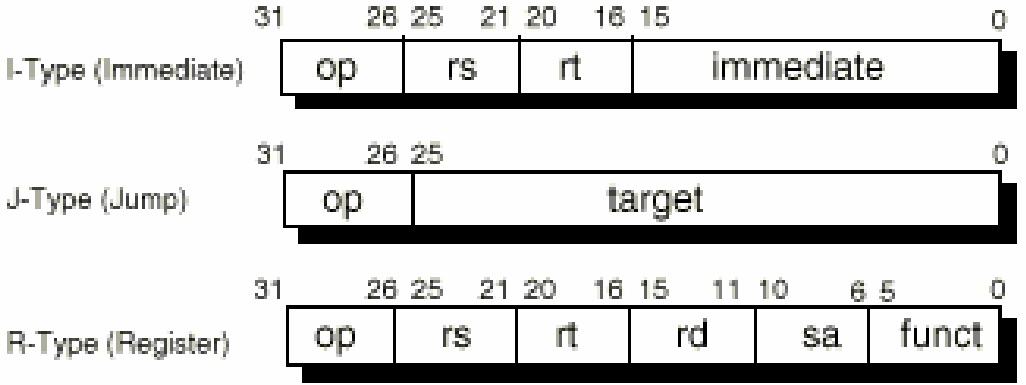
CPU Register Overview

Register width depends on mode of operation: 32-bit or 64-bit

CPU Instruction Set Overview

- Each CPU instruction is 32-bits long.
- There are three instruction formats :
- immediate (I - type)
- jump (J - type)
- register (r - type)

CPU Instruction Set Overview



CPU Instruction Formats

CPU Instruction Set Overview

- Instruction Types :
- Load and store Instructions.
- Computational Instructions.
- Jump and Branch Instructions.
- Special Instructions.
- Exception Instructions.
- Coprocessor Instructions

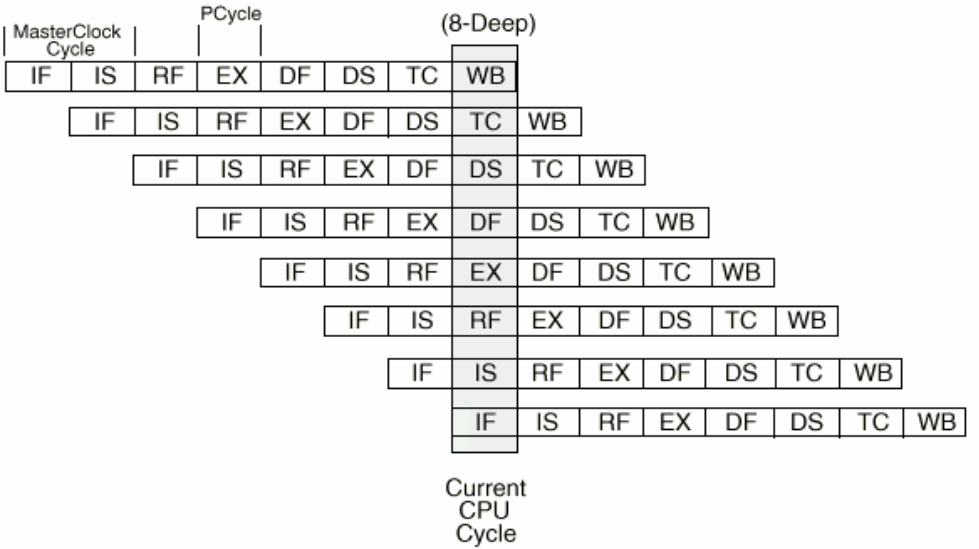
Superpipeline Architecture

- The processor exploits instructions parallelism by using an eight-stage superpipeline which places no restrictions on the instructions issued.
- Under normal circumstances, two instructions are issued each cycle.
- The internal pipeline operates at the twice the frequency of the master clock.

Superpipeline Architecture

- The CPU has an eight-stage instruction pipeline; each stage takes one PCycle. Thus, the execution of each instruction takes at least eight PCycles.
- Once the pipeline has been filled, eight instructions are executed simultaneously.

Superpipeline Architecture



Instruction Pipeline Stages

Superpipeline Architecture

- IF - Instruction Fetch, First half.
- IS - Instruction Fetch, second half.
- RF - Register Fetch.
- EX - Execution.
- DF - Data Fetch, First half.
- DS - Data Fetch, second half.
- TC - Tag check.
- WB - Write Back.

Memory Management Unit(MMU)

- The MIPS R4000 processor provides a full-featured MMU which uses an on-chip translation lookaside buffer(TLB) to translate virtual addresses into physical addresses.

Memory Management Unit(MMU)

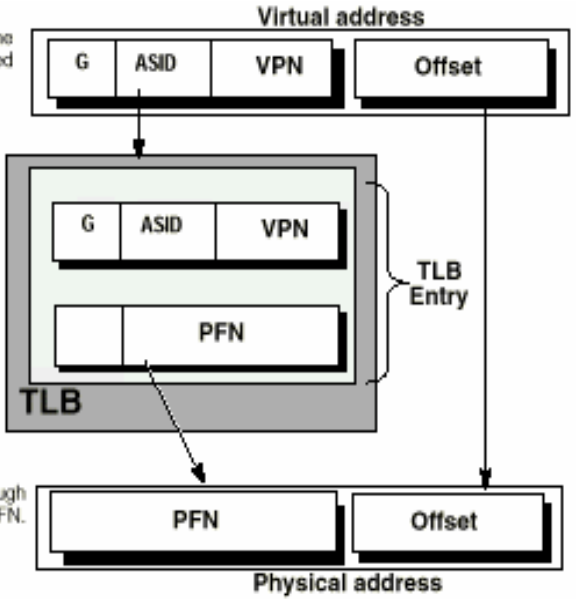
- Translation Lookaside Buffer(TLB):
- Mapped virtual address are translated into physical address using an on-chip TLB. The TLB is a fully associative memory that holds 48 entries. Which provide mapping to 48 odd/even page pairs(96 pages).
- The address mapped to a page ranges in size from 4Kbytes to 16 Mbytes, in multiples of 4 - i.e., 4K, 16K, 256K, 1M, 4M, 16M.

Memory Management Unit(MMU)

- Virtual address space:
- The processor virtual address space can be either 32 or 64 bits wide, depending on whether the processor is operating in 32-bit or 64-bit mode.
- In 32-bit mode, addresses are 32 bits wide. The maximum user process size is 2 Gbytes(231).
- In 64-bit mode, addresses are 64-bits wide. The maximum user process size is 1 Terabyte(240).

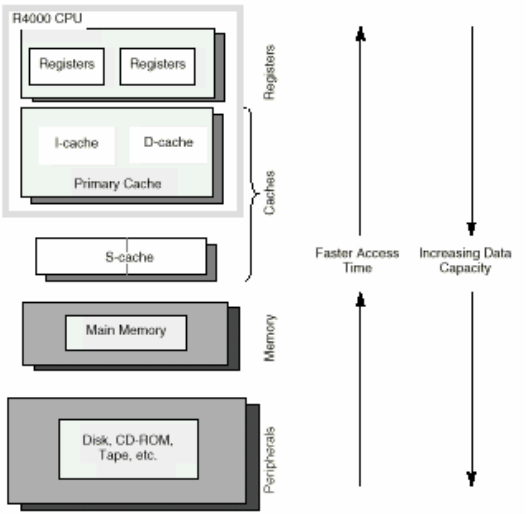
Memory Management Unit(MMU)

1. Virtual address (VA) represented by the virtual page number (VPN) is compared with tag in TLB.
2. If there is a match, the page frame number (PFN) representing the upper bits of the physical address (PA) is output from the TLB.
3. The Offset, which does not pass through the TLB, is then concatenated to the PFN.



Memory Organization

Logical Hierarchy of Memory



Memory Organization

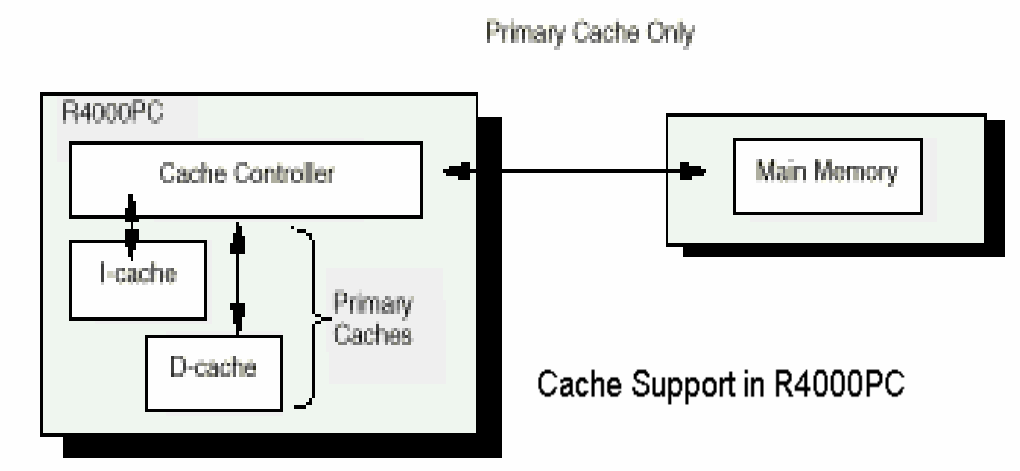
- The R4000 Primary instruction and data caches resides on-chip, and can each hold 8Kbytes. Architecturally, each primary cache can be increased to hold up to 32 Kbytes.
- An off-chip secondary cache (R4000SC and R4000MC only) can hold from 128 Kbytes to 4Mbytes.

Memory Organization

R4000 Cache and Coherency Support

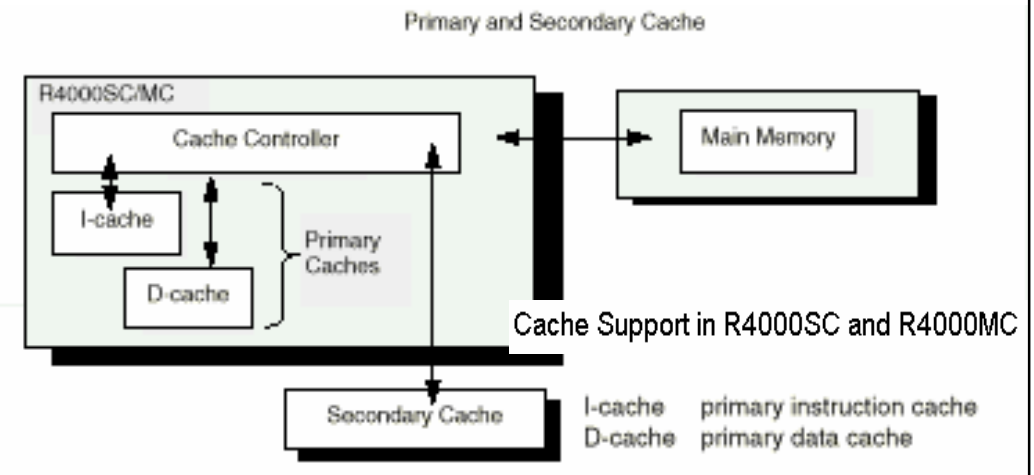
R4000 Model	Support Primary Cache?	Support Secondary Cache?	Support Cache Coherency?
R4000PC	Yes	No	No
R4000SC	Yes	Yes	No
R4000MC	Yes	Yes	Yes

Memory Organization



Cache Support in R4000PC

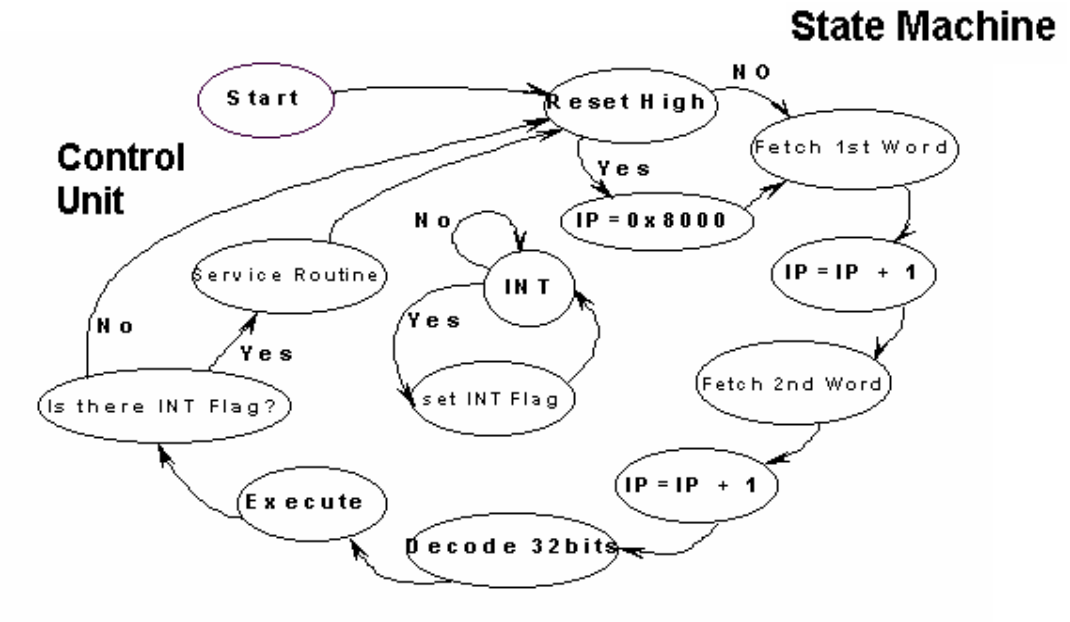
Memory Organization



System Control Coprocessor(CP0)

- CP0 translates virtual addresses into physical addresses and manages exceptions and transitions between kernel, supervisor, and user states.
- CP0 also controls the cache subsystem, as well as providing diagnostic control and error recovery facilities.

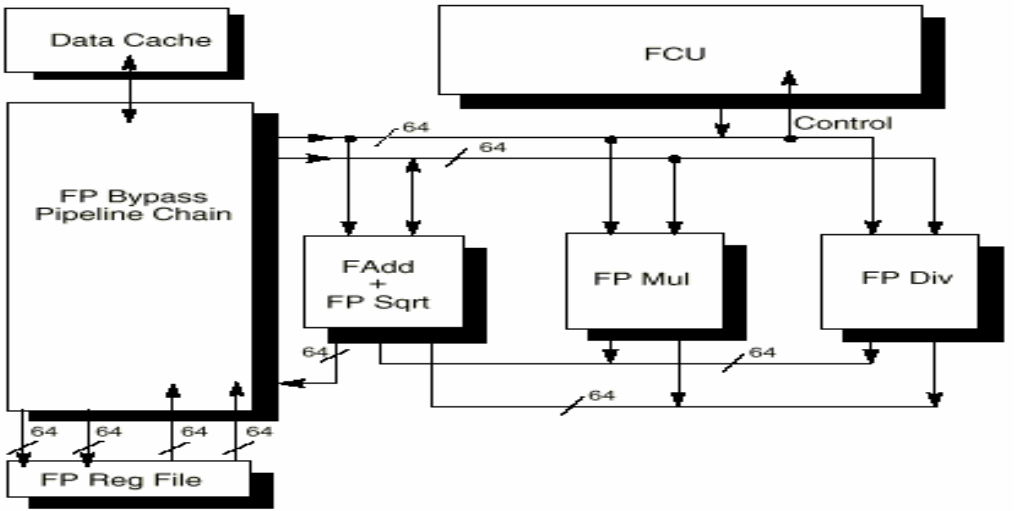
System Control Coprocessor(CP0)



Floating Point Unit(FPU), CP1

- R4000 has on-chip floating point unit designated as CP1. The FPU extends the CPU instruction set to perform arithmetic operations on floating-point values.
- The FPU features include :
- Full 64-bit Operation.
- Load and store instruction set.
- Tightly coupled coprocessor Interface.

Floating Point Unit(FPU)



RISC Vs CISC

- What really distinguishes RISC from CISC these days is more deeply rooted in the chip architectures, among them :
- RISC microprocessors have more general purpose registers.
- RISC microprocessors uses uniform instruction length.
- RISC microprocessors emphasize floating-point performance.

Advantages of RISC

- Speed.
- Simpler hardware.
- Shorter design cycle.
- User(programmer) benefits.

Hazards of RISC

- Code quality.
- Debugging.
- Code expansion.
- System design.

Why RISC ....?

- Which processor will I use ? And how should I choose it ?
- Applications : High speed data transmission,
- Real time processing, controlling applications,..etc.

Remember...!

- Reducing or simplifying the instruction set was not the primary goal of RISC architecture; it is a pleasant side effect of techniques used to gain the highest performance possible from available technology.